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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,048	10/04/2005	Cornelis Hermanus Van Berkel	NL 030348	6163

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EXAMINER
YAARY, MICHAEL D

ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
09/05/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

	Application No.	Applicant(s)
Office Action Summary	10/552,048	VAN BERKEL ET AL.
	Examiner	Art Unit	
	MICHAEL YAARY	2193	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>04 October 2005</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-8</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-8</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>04 October 2005</u> is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some *   c)☐ None of:

        1.☒ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>10/04/2005</u>.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____

5)☐ Notice of Informal Patent Application

6)☐ Other: _____

DETAILED ACTION

1.   Claims 1-8 are pending in the application.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 1, 2, and 4-8 are rejected under 35 U.S.C. 102(b) as being anticipated by

Gu (US Pat. 6,173,009).

4.   **As to claims 1 and 4,** Gu discloses a method for accomplishing state transitions

in configurable linear feedback shift register (LFSR) controlled by a clock (abstract and

column 5, lines 4-5); the length of the LFSR being represented by N, wherein a state

vector represents the state of the LFSR (column 2, lines 11-22 and column 4, lines 61-

67); an output of the LFSR comprising W output symbols, W being at least two, and the

output symbols being generated during one clock cycle (column 3, lines 6-11 and

column 8, lines 19-22), a state transition of the LFSR being accomplished during one

clock cycle via multiplication of the state vector by a state transition matrix to the power

of W, characterized in that said multiple state transition matrix is decomposed in a first matrix and a second matrix, the first matrix comprising at most N+W+1 different expressions and the second matrix comprising at most N+W+1 different expressions (column 3, lines 6-54 and column 4, line 55-column 5, line 36).

5.   **As to claims 2 and 7,** Gu discloses wherein the expressions of the first matrix are evaluated during a configuration stage of the operation of the LFSR (column 5, lines 15-36).

6.   **As to claim 5,** Gu discloses that the multiplication means comprises a first set of logical units for performing the multiplication of the state vector by the second matrix and a second set of logical units for performing the multiplication of the state vector by the first matrix (column 5, lines 15-36 and different multiplication stages of figure 6).

7.   **As to claim 6,** Gu discloses that the LFSR comprises a third set of logical units for computing the first matrix (column 5, lines 15-36).

8.   **As to claim 8,** Gu discloses the second set of logical units is coupled to the first set of logical units via an intermediate data register (column 2, line 57-column 3, line 8).

Claim Rejections - 35 USC § 103

9.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10.   Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu.

11.   Gu does not explicitly define the second matrix elements by $Gij=\{1$, if $i-j=W$; $gi+j-N+1$, if $(i+j)>=N-1)$ ^ $(j>=N-W)$; 0, otherwise and the elements of the first matrix are defined $Pij=\{1$, if $i=j$ ^ $i<N-W$; $Pi+j-2N+W+1$, if $I+j>=2N-W-1$; 0, otherwise.

Howeve, Gu discloses defining matrix elements used in the circuit LFSR circuit producing state transitions (column 4, line 32-column 5, line 67).

12.   Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the matrices implemented in the circuit, as taught by Gu, for the benefit of obtaining the predictable result of state transitions. Further motivation can be found in that the matrices defined in Gu would allow for minimal memory storage requirements for transition matrices.

Conclusion

13.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

       US Pat. 5,987,056 - PN sequence hopping method and system

       US Pat. 6,594,680 - Pseudo-random noise sequence generating system

       US Pat. 6,640,236 – Generating multiple bits of a pseudo-noise sequence

       Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MICHAEL YAARY whose telephone number is

(571)270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m -

5:00 p.m..

       If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

       Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. Y./
Examiner, Art Unit 2193

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193